WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a non-volatile memory element;

a latch circuit which latches data read from the non-volatile memory element;

a control circuit which requires the data latched in the latch circuit; and

a decoder which is connected to a transfer path of the data extending from the non-volatile memory element to the control circuit, and decodes the data.

2. The semiconductor integrated circuit according to claim 1, wherein the data read from the non-volatile memory element is encoded data, and the decoder decodes the data immediately after being read from the non-volatile memory element.

3. The semiconductor integrated circuit according to claim 1, wherein the data read from the non-volatile memory element is encoded data, and the decoder decodes the data immediately before being inputted to the latch circuit.

4. The semiconductor integrated circuit according to claim 1, wherein the data read from the non-volatile memory element is encoded data, and the decoder decodes the data immediately after being outputted from the latch circuit.

5. The semiconductor integrated circuit according to claim 1, wherein the transfer path is constituted of

a shift register, and the data is transferred in serial.

6. The semiconductor integrated circuit according to claim 1, wherein the decoder has a function to detect an error in the data and correct the error in the data.

7. A semiconductor integrated circuit comprising:

a non-volatile memory element;

a latch circuit which latches data read from the non-volatile memory element;

a control circuit which requires the data latched in the latch circuit;

an encoder which is connected to a transfer path of the data extending from the non-volatile memory element to the control circuit, and encodes the data; and

a decoder which is connected to the transfer path, and decodes the data encoded by the encoder.

8. The semiconductor integrated circuit according to claim 7, wherein the encoder encodes the data immediately after being read from the non-volatile memory element, and the decoder decodes the data immediately before being inputted to the latch circuit.

9. The semiconductor integrated circuit according to claim 7, wherein the encoder encodes the data immediately after being read from the non-volatile memory element, and the decoder decodes the data

immediately after being outputted from the latch circuit.

10. The semiconductor integrated circuit according to claim 7, wherein the encoder encodes the data immediately before being inputted to the latch circuit, and the decoder decodes the data immediately after being outputted from the latch circuit.

11. The semiconductor integrated circuit according to claim 7, wherein the transfer path is constituted of a shift register, and the data is transferred in serial.

12. The semiconductor integrated circuit according to claim 7, wherein the decoder has a function to detect an error in the data and correct the error in the data.

13. A semiconductor integrated circuit comprising:

a non-volatile memory element;

an encoder which encodes data read from the non-volatile memory element;

a latch circuit which latches the data encoded by the encoder;

a decoder which decodes the data latched in the latch circuit; and

a control circuit which requires the data decoded by the decoder.

14. The semiconductor integrated circuit according to claim 13, wherein the decoder has a function to

detect an error in the data and correct the error in the data.

15. The semiconductor integrated circuit according to claim 14, further comprising a latch data refresh control circuit which controls the latch circuit,

wherein the latch data refresh control circuit again latches the data error-corrected by the decoder in the latch circuit when the decoder detects an error in the data.

16. The semiconductor integrated circuit according to claim 15, wherein the error-corrected data is decoded, and then again latched in the latch circuit through the encoder.

17. The semiconductor integrated circuit according to claim 15, wherein the error-corrected data is again latched in the latch circuit without being decoded.

18. The semiconductor integrated circuit according to claim 14, further comprising a transfer control circuit which controls transfer of the data read from the non-volatile memory element,

wherein, when the decoder detects an error in the data and the data is beyond an error correction capability of the decoder, the transfer control circuit again transfers the data read from the non-volatile memory element to the latch circuit.

19. A setting method of a chip initial state comprising:

programming data in a non-volatile memory element;

encoding the data read from the non-volatile memory element and latching it in a latch circuit;

decoding the data latched in the latch circuit;

correcting an error in the data upon detecting the error in the data when decoding the data, and again latching the error-corrected data in the latch circuit; and

performing basic setting concerning operations of internal circuits based on the error-corrected data.

20. The setting method according to claim 19, wherein, in case of decoding the data, when an error in the data is detected and the error is beyond an error correction capability, the data read from the non-volatile memory element is again transferred to the latch circuit.